22. (Original) The apparatus as recited in claim 9, the computer readable program code devices of the compact flash controller continues to perform each of the data transfer operative elements until the data transfer is complete.

23. (Previously presented) The computer program product as recited in claim 17, the computer readable program code devices of the compact flash controller stands by waiting for a predetermined time period for the next data transfer operation.

24. (Original) The computer program product as recited in claim 23, the computer readable program code devices of the compact flash controller suspends any operative activity and waits until a request to execute a new command sequence to be detected, if the a predetermined time period elapses.

* * * R*E*M*A*R*K*S * * *

Applicants herewith submit this Response C in a bona fide attempt to advance the prosecution of this case and to answer each and every ground of rejection as set forth by the Examiner. Applicants respectfully request reconsideration of the above referenced patent application in view of the remarks as set forth below.

Rejections under 35 U.S.C. §103

The Examiner has rejected claims 1 through 24 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent Application Publication No. US 2003/0009607 A1 published on January 9, 2003 by Joe Chen (Chen) in view of United States Patent Application Publication No. US 2001/0007119 A1 published on July 5, 2001 to Kunihiro Katayama et al. (Katayama et al.) and further in view of United States Patent Application Publication No. US 2003/0033465 A1 published on February 13, 2003 by Cheng-Chih Chien et al. (Chien et al.).

Applicants submit that neither Chen nor Chien et al are valid prima facie references. The Chen and Chien et al. references were both published on January 9,

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2003 and February 13, 2003, respectively, after the filing date of Applicants' claimed invention. Therefore neither reference is permissible as a §103 reference. Unless the Examiner has evidence that either or both references were known by Applicant prior to the filing date of the instant application, they must each be withdrawn at once. In any case, neither reference anticipates, teaches or even suggests Applicant's claimed invention as noted below.

In rejecting claims 1, 9 and 17 the Examiner states "...Chen teaches a flash system ... in which ... controller ... initiates the functionally of ... components, processes ... commands ... and executes transfers of data .... Chen does not teach a flash memory ... of flash memory arrays ... partitioning ... memory arrays, or ... transfer of data to a memory array pair ....". The Examiner further states " ... Katayama et al. teaches a file memory ... with ... memory arrays ... organized in ... parallel ... memory element groups ... data ... distributed through out the arrays through ... use of ... data distribution unit ... transferring data to a memory array pair ....".

The Examiner continues to state "... memory groups 'a' and 'b' ... make up the memory array pair ... obvious ... to integrate ... memory partitioning and data transferring method of Katayama et al. with ...Chen ... to give the system ... ability of interleaving data throughout ... arrays ....". The Examiner states "... Chen and Katayama et al does not disclose ... controller configured to partition ... arrays ... of ... information table stored in a memory of ... flash controller. Chien et al. discloses IDE system in which an IDE controller ... comprises a memory ... and reads from its memory a partition table ... and provides information from ... table ...to create virtual partitions in ... disk drive .... Chien discloses ... disk drive ... could be a flash memory storage device ... obvious ... to integrate ... table of Chien et al. with combined system of Chen and Katayama et al. ....".

The Examiner further states " Regarding Claims 2-3, 10-11, and 18-19, Chen teaches ... what interface to use .... Regarding Claims 4, 12 and 20, Chen teaches ... host provides ... write command ... interpreted by the controller ... to .... write data

from the controller into ...ROM .... Regarding Claims 5, 13 and 21, Chen teaches a system in which the host provides ... controller ... a read command ... to read data from ...ROM and store it in a RAM .... Regarding Claims 6, 14 and 22, Chen teaches ... number of bytes ... to be transferred .... Regarding Claims 7-8, 15-16, and 23-24 Chen's flash controller does not perform any write, read, or transfer operation until a command is received from the host.".

In Response to Arguments, the Examiner states "... Chien et al. teaches the elements not taught by Chen in view of Katayama. Katayama et al teaches a file memory device ... divided into memory arrays ... organized in a parallel arrangement of memory element groups ... memory control circuit 28 controls ... flash memory 5, however it does not control the partitioning of the flash memory. Chien et al. discloses an IDE controller, which stores ... a partitioning table ....". Applicants respectfully traverses the Examiner's rejection of applicants' claims 1 through 24.

It is respectfully submitted that even a 35 U.S.C. § 102 rejection of applicants' claims 1 through 24 does not apply in that the cited references of Chen, Katayama et al. and Chien et al. do not disclose, teach or anticipate the novel structure and method recited in applicants' claims 1 trough 24.

Even if a 35 U.S.C. §103 rejection were appropriate, the Examiner admits that applicant's claims 1 through 24 are not obvious with regard to Chen in view of Katayama et al. Even the Examiner admits that the combination of Chen and Katayama et al. do not disclose a flash controller configured to partition flash memory arrays in accordance with parameters of a configuration stored in a memory of the flash controller. Chien et al. does not as is recited by applicants' claim 1 a method for "... determining which interface specification is to be used to transfer data, address information and control signals to and from a host device ...". A careful review of the apparatus disclosed by Chien el al. fails to disclose how they would accomplish this feature of applicants' novel invention. Nor is this feature of applicants' invention obvious from Chen in view of Katayama et al. and Chien et al. Even the large number

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of references cited by the Examiner does not render applicants' method , circuitry or computer readable code recited by claims 1, 9 and 17 obvious.

In addition, a careful review of Chien et al. does not, contrary to the Examiner's remarks, reveal detecting a plurality of memory arrays. The drawing and specification by Chien et al. only disclose typical disk drive and flash memory storage devices. Since there are no memory arrays in Chien et al it cannot possibly teach how partition them. Chien et al. does not teach how to determine which interface specification is to be used. In fact, there is nothing remotely in Chien et al to lead one to believe that structure is of any consideration or of value in Chien et al. It appears to the undersigned that Chien et al. needs both and cannot make a selection.

Additionally, Chien et al. does not teach how to translate the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair. Further there is no suggestion, let alone teaching on how the ATA system adapter taught by Chien et al would be connected with the apparatus of Takayama et al. Perhaps the Examiner can, in the next office action, point out to the Applicant where that language is, either in Takayama et al or in Chien et al. Since there is no such teaching, it is respectfully submitted that the Examiner is using impermissible hindsight and in fact using Applicants' own disclosure, as the teaching to hold together the hypothetical combination. This clearly is impermissible and the rejection for these the other reasons mentioned above and below should be immediately withdrawn.

Even if were possible to combine Chen, Takayama et al. and Chien et al., without using the Applicants' own disclosure, that hypothetical combination would still not render obvious Applicants' claimed invention. Specifically the method, circuitry or computer readable code recited in claims 1, 9 and 17 for detecting the number of compact flash memory arrays that comprise the compact flash memory device; initializing a plurality of flash memory arrays; partitioning each of the flash memory

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arrays in accordance to the parameters of a configuration information table stored in a read-only memory of the compact flash controller; and translating the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair are not taught, anticipated or even suggested by the hypothetical combination.

Please note that Chien et al. alleges, paragraph 0021, a virtual partition table cooperative with hot swap devices under standard industrial regulations. Standard storage devices such as disk drives utilize tables to select disk segments to store information. Yet the combination of Chen, Takayama et al. and Chien et al. do not render obvious applicants' method, circuitry or computer readable code recited in claims 1, 9 and 17 for partitioning each of the flash memory arrays in accordance to the parameters of a configuration information table stored in a read-only memory of the compact flash controller and translating the specified command sequence into a set of data transfer operative elements that provide for the transfer of data to a corresponding memory array pair. One must ask how would these claimed features be obvious of Chen in view of Katayama et al. and Chien et al. especially since the Chen and Chien et al. references were not available when applicants application was filed and even if the combination of Chen, Katayama et al. and Chien et al had been available.

It is respectfully submitted that independent claims 1, 9 and 17 and dependent claims 2 through 8, 10 through 16 and 18 through 24, further defining the method, circuitry and computer readable program code devices of parent claims 1, 9 and 17 respectively, are non-obvious in view of and particularly distinguish over Chen, Takayama et al. and Chien et al. references and claims 1 through 24 are clearly allowable under 35 U.S.C. 103 in accordance with the principles of Graham vs. John Deere Co.

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CONCLUSION

In summary, applicants have again reviewed the specification, drawing and claims and believe they are in condition for allowance. The Examiner has again rejected claims 1 through 24. In view of the arguments herein set forth, applicants respectfully submit that claims 1 through 24 distinguish over the art cited by the Examiner and are allowable. Applicant having answered each and every ground of rejection as set forth by the Examiner submits that the case is in condition for allowance and the same is respectfully solicited. Favorable action in that regard and passage of this case to issue are earnestly solicited.

If any questions should arise with respect to the above remarks, or if it would in any way expedite the prosecution of this case, applicants' attorney would appreciate a telephone call by dialing Area Code (408)-965-4001.

Respectfully submitted,

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